

ME310G1 Hardware Design Guide

1VV0301588 Rev. 3 - 2019-10-08





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APPLICABILITY TABLE

PRODUCTS

ME310G1-W1

■ ME310G1-WW



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1. INTRODUCTION

1.1. Scope

This document introduces the ME310G1 module and presents possible and recommended hardware solutions for developing a product based on this module. All the features and solutions detailed in this document are applicable to all the variants listed in the applicability table.

Obviously, this document cannot embrace every hardware solution or every product that can be designed. Where the suggested hardware configurations need not be considered mandatory, the information given should be used as a guide and a starting point for properly developing your product with the Telit module.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our ME310G1 modules.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Text Conventions



Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.



Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.



Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.5. Related Documents



2. GENERAL PRODUCT DESCRIPTION

2.1. Overview

The ME310G1 module is a CATM / NBIoT communication product which allows integrators to plan on availability for even the longest lifecycle applications, highly recommended for new designs specified for coverage worldwide.

The product is fully voice capable, the analog and digital audio interfaces make it suitable for applications such as voice enabled alarm panels, mHealth patient monitors and specialty phones such as those for the elderly or sensory-impaired.

The ME310G1 operates with 1.8 V GPIOs, minimizing power consumption and making it even more ideally suited for battery powered and wearable device applications.

2.2. Product Variants and Frequency Bands

| Product | 2G Band (MHz) | LTE CATM1 | NBIoT | Region |
|------------|-------------------------|--|--------------------------------|-----------|
| ME310G1-W1 | - | B1, B2, B3, B4, B5, B8, B12, B13, B18, B19, B20, B25, B26, B27, B28, B66, B85 | B5, B8, B12, B13, B18, B19, | Worldwide |
| ME310G1-WW | 850, 900, 1800, 1900 | B1, B2, B3, B4, B5, B8, B12, B13, B18, B19, B20, B25, B26, B27, B28, B66, B85 | B5, B8, B12, B13, B18, B19, | Worldwide |

Refer to "RF Section" for details information about frequencies.



NOTE:

Cellular technologies and frequency bands that are enabled may vary based on firmware version and firmware configuration used.



2.3. Target Market

ME310G1 can be used for telematics applications where tamper-resistance, confidentiality, integrity, and authenticity of end-user information are required, for example:

- Telematics services
- Road pricing
- Pay-as-you-drive insurance
- Stolen vehicles tracking
- Internet connectivity

2.4. Main features

| Function | Features |
|------------|---|
| Modem | CATM and NBIoT technologies SMS support (text and PDU) Alarm management Real Time Clock |
| Interfaces | Main UART for AT command access Secondary UART and SPI interfaces for general purpose use AUX UART used for diagnostic monitoring and debugging SPI 6 GPIOs Antenna port |



2.5. TX Output Power

ME310G1-W1

| Band | Mode | Class | RF power (dBm) |
|---|-------------------|-------|----------------|
| B1, B2, B3, B4, B5, B8, B12, B13, B14, B18, B19, B20, B25, B26, B27, B28, B66, B85 | (LTE) CAT- M1 | 5 | 20 (+-2dB) |
| B1, B2, B3, B4, B5, B8, B12, B13, B18, B19, B20, B25, B26, B28, B66, B71, B85 | (LTE) CAT- NB1 | 5 | 20 (+-2dB) |

ME310G1-WW

| Band | Mode | Class | RF power (dBm) |
|--|-------------------|-------|----------------|
| 850/900MHz | GSM | 4 | 33 (+-2dB) |
| 1800/1900MHz | DCS/PCS | 1 | 30 (+-2dB) |
| B1, B2, B3, B4, B5, B8, B12, B13, B14, B18, B19, B20, B25, B26, B27, B28, B66, B85 | (LTE) CAT- M1 | 3 | 23 (+-2dB) |
| B1, B2, B3, B4, B5, B8, B12, B13, B18, B19, B20, B25, B26, B28, B66, B71, B85 | (LTE) CAT- NB1 | 3 | 23 (+-2dB) |

2.6. RX Sensitivity

This section will be available in next document revisions.

2.7. Mechanical Specifications

2.7.1. Dimensions

The overall dimensions of ME310G1-W1 are:

Length: 14.3 mmWidth: 13.1 mmThickness: 2.6 mm

The overall dimensions of ME310G1-WW are:

Length: 15.0 mmWidth: 18.0 mmThickness: 2.6 mm

2.7.2. Weight

The nominal weight of the ME310G1-W1 is 1 gram.

The nominal weight of the ME310G1-WW is 1.5 grams.



2.8. Temperature Range

| | | Note |
|--------------------------------|----------------|---|
| Operating Temperature Range | –20°C to +55°C | The module is fully functional(*) within this 3GPP temperature range and meets 3GPP specifications. |
| Extended Temperature Range | –40°C to +85°C | The module is fully functional (*) within this temperature range. The RF performance may deviate from 3GPP requirements in this extended range. For example: receiver sensitivity or maximum output power may deviate by a few dB due to limitations of physics like higher thermal noise floor at high temperature. |
| Storage Temperature Range | –40°C to +85°C | - |

^(*) Functional: if applicable, the module is able to make and receive voice calls, data calls, send and receive SMS and data traffic.



3. PINS ALLOCATION

3.1. Pin-out

| Pin | Signal | I/O | Function | Туре | Comment | | | |
|---------|---|--------|---|-----------|---------|--|--|--|
| Asynch | Asynchronous Serial Port (USIF0) – Prog. / Data + HW Flow Control | | | | | | | |
| Y16 | TXD0 | I | Serial data input (TXD) from DTE | CMOS 1.8V | | | | |
| AA15 | RXD0 | 0 | Serial data output (RXD) to DTE | CMOS 1.8V | | | | |
| Y18 | RTS0 | I | Input for Request to send signal (RTS) from DTE | CMOS 1.8V | | | | |
| AA17 | CTS0 | 0 | Output for Clear to send signal (CTS) to DTE | CMOS 1.8V | | | | |
| Asynch | nronous Serial P | ort (U | SIF1) | | | | | |
| Y12 | TXD1 | 1 | Serial data input (TXD) from DTE | CMOS 1.8V | | | | |
| AA11 | RXD1 | 0 | Serial data output (RXD) to DTE | CMOS 1.8V | | | | |
| AA13 | RTS1 | I | Input for Request to send signal (RTS) from DTE | CMOS 1.8V | | | | |
| Y14 | CTS1 | 0 | Output for Clear to send signal (CTS) to DTE | CMOS 1.8V | | | | |
| USB H | S 2.0 COMMUNIC | CATIC | ON PORT | | | | | |
| U19 | USB_D+ | I/O | USB differential Data (+) | | | | | |
| V18 | USB_D- | I/O | USB differential Data (-) | | | | | |
| T18 | USB_VBUS | - | Power sense for the internal USB transceiver | | | | | |
| Auxilia | ry Serial Port | | | | | | | |



| Y10 | TX_AUX | 0 | Auxiliary UART (TX Data to DTE) | CMOS 1.8V | | | | |
|--------|--------------------|-----|---------------------------------|-----------|---------------------------------------|--|--|--|
| AA9 | RX_AUX | I | Auxiliary UART (RX Data to DTE) | CMOS 1.8V | | | | |
| SIM ca | SIM card interface | | | | | | | |
| L1 | SIM_CLK | 0 | External SIM signal – Clock | CMOS 1.8V | | | | |
| M2 | SIM_RST | 0 | External SIM signal – Reset | CMOS 1.8V | | | | |
| N1 | SIM_DAT | I/O | External SIM signal – Data I/O | CMOS 1.8V | | | | |
| P2 | SIM_VCC | - | Power supply for the SIM | 1.8V | Only 1.8V simcard are supported | | | |
| Х | SIMIN | I | Presence SIM input | CMOS 1.8V | See next chapters | | | |
| SPI | | | | | | | | |
| AA5 | SPI_MOSI | I/O | SPI MOSI | CMOS 1.8V | | | | |
| Y8 | SPI_MISO | I/O | SPI MISO | CMOS 1.8V | | | | |
| AA7 | SPI_CLK | I/O | SPI Clock | CMOS 1.8V | | | | |
| Y6 | SPI_CS | I/O | SPI Chip Select | CMOS 1.8V | | | | |
| DIGITA | AL IO | | | | | | | |
| V11 | IO1 | I/O | Configurable GPIO01 | CMOS 1.8V | | | | |
| V13 | IO2 | I/O | Configurable GPIO02 | CMOS 1.8V | | | | |
| D7 | IO3 | I/O | Configurable GPIO03 | CMOS 1.8V | | | | |
| D9 | 104 | I/O | Configurable GPIO04 | CMOS 1.8V | | | | |
| | | | | | | | | |



| D11 | 105 | I/O | Configurable GPIO05 | CMOS 1.8V | DTR is alternate function |
|--------|----------------------|-----|---|-----------|----------------------------------|
| D13 | 106 | I/O | Configurable GPIO06 | CMOS 1.8V | RING is alternate function |
| ADC a | nd DAC | | | | |
| B18 | ADC | I | Analog To Digital converter Input | A/D | |
| R16 | DAC | 0 | Digital To Analog converter Output | D/A | PWM signal |
| RF Sec | ction | | | | |
| A5 | CELL_MAIN ANTENNA | I/O | Main Antenna (50 ohm) | RF | |
| E19 | GNSS ANTENNA | I | GNSS Antenna | RF | |
| GNSS | Control Signals | | | | |
| H18 | GNSS_LNA_E N | 0 | GNSS external LNA enable | CMOS 1.8V | |
| G16 | GNSS_PPS | 0 | 1 Pulse per Second | CMOS 1.8V | |
| Miscel | laneous Function | ns | | | |
| B2 | S_LED | 0 | Status LED | CMOS 1.8V | |
| N16 | ON_OFF*/WA KE* | I | Input Command for Power ON/OFF and to wake from deep sleep mode | CMOS 1.8V | Active Low |
| R1 | PWRMON | 0 | Power ON Monitor | CMOS 1.8V | |
| N4 | CTANK | - | Internal supply domain pin for external tank capacitor | 1.8V | |
| | | | | | |



| T2 | FORCED_USB_ BOOT | I | Optional pin, connect to test point | CMOS 1.8V | Active high, internal PD (100K) | | | | |
|-------|---------------------|-----|-------------------------------------|-----------|---------------------------------------|--|--|--|--|
| Audio | Audio Section | | | | | | | | |
| C1 | DVI_WA0 | I/O | Digital Audio Interface (WA0) | CMOS 1.8V | | | | | |
| D2 | DVI_RX | 0 | Digital Audio Interface (RX) | CMOS 1.8V | | | | | |
| E1 | DVI_TX | I | Digital Audio Interface (TX) | CMOS 1.8V | | | | | |
| F2 | DVI_CLK | I | Digital Audio Interface (CLK) | CMOS 1.8V | | | | | |
| Power | Supply | | | | | | | | |
| W1 | VBATT_PA | - | Main power supply (Radio PA) | Power | | | | | |
| AA3 | VBATT | - | Main power supply (Baseband) | Power | | | | | |
| A3 | GND | - | RF Ground | Power | | | | | |
| A7 | GND | - | RF Ground | Power | | | | | |
| A9 | GND | - | RF Ground | Power | | | | | |
| A13 | GND | - | RF Ground | Power | | | | | |
| A17 | GND | - | RF Ground | Power | | | | | |
| B4 | GND | - | RF Ground | Power | | | | | |
| В6 | GND | - | RF Ground | Power | | | | | |
| B10 | GND | - | RF Ground | Power | | | | | |
| B12 | GND | - | RF Ground | Power | | | | | |
| B14 | GND | - | RF Ground | Power | | | | | |



| | | | | 1 |
|-----|-----|---|----------------|-------|
| B16 | GND | - | RF Ground | Power |
| C19 | GND | - | RF Ground | Power |
| D18 | GND | - | RF Ground | Power |
| F8 | GND | - | Thermal Ground | Power |
| F12 | GND | - | Thermal Ground | Power |
| F18 | GND | - | Thermal Ground | Power |
| G19 | GND | - | Thermal Ground | Power |
| H6 | GND | - | Thermal Ground | Power |
| H14 | GND | - | Thermal Ground | Power |
| J19 | GND | - | Thermal Ground | Power |
| K18 | GND | - | Thermal Ground | Power |
| M18 | GND | - | Thermal Ground | Power |
| N19 | GND | - | Thermal Ground | Power |
| P6 | GND | - | Thermal Ground | Power |
| P14 | GND | - | Thermal Ground | Power |
| Т8 | GND | - | Thermal Ground | Power |
| T12 | GND | - | Thermal Ground | Power |
| U1 | GND | - | Power Ground | Power |
| V2 | GND | - | Power Ground | Power |
| W19 | GND | - | Power Ground | Power |
| | | | | |



| Y2 | GND | - | Power Ground | Power |
|-------|----------|---|--------------|-------|
| Y4 | GND | - | Power Ground | Power |
| RESER | VED | | | |
| G1 | RESERVED | - | RESERVED | |
| H2 | RESERVED | - | RESERVED | |
| J1 | RESERVED | - | RESERVED | |
| K2 | RESERVED | - | RESERVED | |
| J4 | RESERVED | - | RESERVED | |
| G4 | RESERVED | - | RESERVED | |
| L19 | RESERVED | - | RESERVED | |
| A11 | RESERVED | - | RESERVED | |
| R4 | RESERVED | - | RESERVED | |
| L4 | RESERVED | - | RESERVED | |
| V7 | RESERVED | - | RESERVED | |
| V9 | RESERVED | - | RESERVED | |
| L16 | RESERVED | - | RESERVED | |
| P18 | RESERVED | - | RESERVED | |
| J16 | RESERVED | - | RESERVED | |
| R19 | RESERVED | - | RESERVED | |
| В8 | RESERVED | - | RESERVED | |



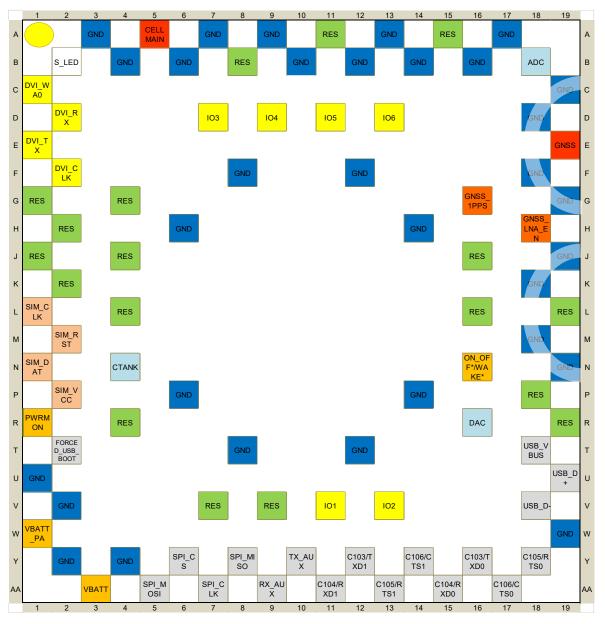


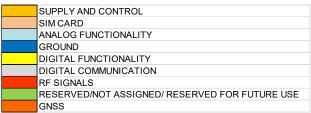
WARNING:

Reserved pins must not be connected.

3.2. LGA Pads Layout

TOP VIEW







4. POWER SUPPLY

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

4.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfil the following requirements:

| Power Supply | Value |
|-------------------------|-----------------|
| Nominal Supply Voltage | 3.8V |
| Operating Voltage Range | 3.40 V - 4.20 V |
| Extended Voltange Range | 2.60 V - 4.50 V |
| VBATT _{min} | 2.60V |



CAUTION:

The range 2.60V - 3.20V can be used only if both USB and 2G are disabled.



NOTE:

The Operating Voltage Range MUST never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop. If the voltage drop is exceeding the limits it could cause a Power Off of the module.

Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded.



NOTE:

For PTCRB approval on the final products the power supply is required to be within the "Normal Operating Voltage Range".



4.2. Power Consumption

Preliminary data

| Mode | Average (mA) | Mode Description |
|--------------------------|--------------|---|
| IDLE MODE | | |
| AT+CFUN=1 | 8 | Normal mode: full functionality of the module |
| AT LOCUME | 0.98* | Paging cycle #256 frames (2.56s DRx cycle) |
| AT+CFUN=5 | 0.47* | 81.92s eDRx cycle length (PTW=2.56s, DRX=1.28s) |
| PSM MODE | | |
| AT+CPSMS=1 3uA | | No current source or sink by any connected pin |
| OPERATIVE MOD | E | |
| LTE CAT M1 Data Call | 105 | TX=0dBm, BW=10MHz, Max Throughput 375Kbps (DL) |
| LTE CAT NB1 Data Call | 49 | TX=0dBm |

^{*}Based on chipset vendor reference data



NOTE:

The reported LTE CAT M1 and LTE CAT NB1 values are an average among all the product variants and bands for each network wireless technology.

The support of specific network wireless technology depends on product variant configuration.



4.3. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout

4.3.1. Electrical Design Guidelines

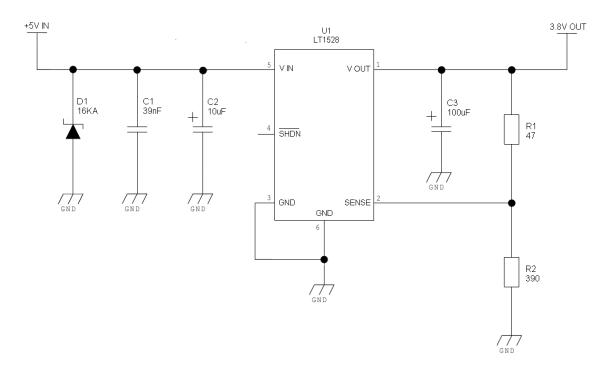
The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

4.3.1.1. +5V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used.
 A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the Module, a 100µF capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output rated at least 10V.

An example of linear regulator with 5V input is:

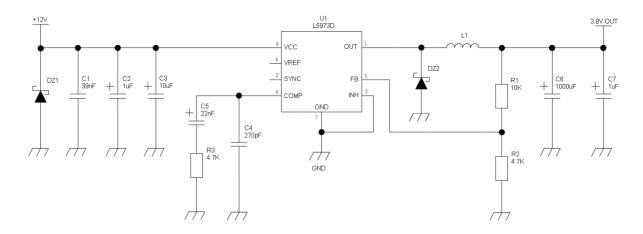




4.3.1.2. +12V Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.

An example of switching regulator with 12V input is in the below schematic:



4.3.1.3. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, hence a single 3.7V Li-lon cell battery type is suited for supplying the power to the Telit ME310G1 module.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the ME310G1 from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery must be rated to supply peaks of current up to 2A.





NOTE:

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with ME310G1. Their use can lead to overvoltage on the ME310G1 and damage it. USE ONLY Li-Ion battery types.

4.3.2. Thermal Design Guidelines

This section will be available in next document revisions.

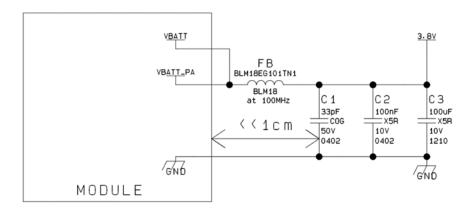


4.3.3. Power Supply PCB layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks on the input to protect the supply from spikes The placement of this component is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performance.

- The Bypass low ESR capacitor must be placed close to the Telit ME310G1 power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the ME310G1 is wide enough to ensure a dropless connection even during an 2A current peak.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces to the ME310G1 and the Bypass capacitor must be wide enough to
 ensure no significant voltage drops occur. This is for the same reason as previous
 point. Try to keep this trace as short as possible.
- To reduce the EMI due to switching, it is important to keep very small the mesh involved; thus the input capacitor, the output diode (if not embodied in the IC) and the regulator have to form a very small loop. This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- A dedicated ground for the Switching regulator separated by the common ground plane is suggested.
- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.
- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines. A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

The below figure shows the recommended circuit:





4.4. RTC

RTC is functional when ME310G1 is in PSM or OFF state and VBATT pin is supplied. RTC settings are erased if VBATT supply is temporary disconnected.

4.5. PWRMON Power-on monitor

PWRMON is always active (output high) when the module is powered ON (module powered ON indication) and cannot be set to LOW level by any AT command.

This signal is present on pin R1. The operating range characteristics of PWRMON signal are:

| Item | Min | Typical | Max |
|----------------|-------|---------|-----|
| Output voltage | 1.35V | 1.8V | - |
| Output current | - | - | 1mA |



If PSM is enabled by AT+CPSMS

Command, PWRMON during PSM period is LOW



NOTE:

The Output Current MUST never be exceeded; care must be taken when designing the application section to avoid having an excessive current consumption.

If the Current is exceeding the limits it could cause a Power Off of the module.



WARNING:

This signal is NOT provided in order to supply small devices from the module. PWRMON is only a module power-on indicator.



5. DIGITAL SECTION

ME310G1 has four main operation states:

- **OFF state:** Vbatt is applied and only RTC is running. Baseband is switched OFF and the only change possible is the ON state.
- **ON state:** baseband is fully switched on and ME310G1 is ready to accept AT commands. ME310G1 can be idle or connected.
- Sleep mode state: main baseband processor is intermittently switched ON and AT commands can be processed with some latency. ME310G1 is idle with low current consumption.
- **Deep sleep mode state:** PSM defined in 3GPP Release 12. Baseband is switched OFF most of the time.

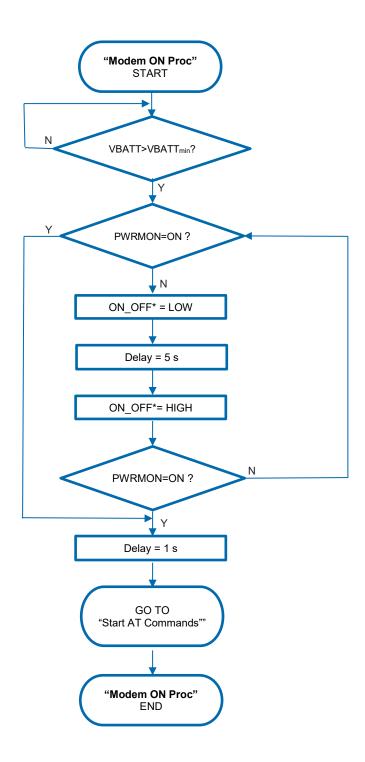
5.1. Logic Levels

| Parameter | Min | Max |
|--|-------|-------|
| ABSOLUTE MAXIMUM RATINGS – NOT FUNCTIONAL | | |
| Input level on any digital pin (CMOS 1.8) with respect to ground | -0.3V | 2.1V |
| Operating Range - Interface levels (1.8V CMOS) | | |
| Input high level | 1.5V | 1.9V |
| Input low level | 0V | 0.35V |
| Output high level | 1.6V | 1.9V |
| Output low level | 0V | 0.2V |

| Parameter | AVG |
|--------------------------|-----|
| CURRENT CHARACTERISTICS: | |
| Output Current | 1mA |
| Input Current | 1uA |

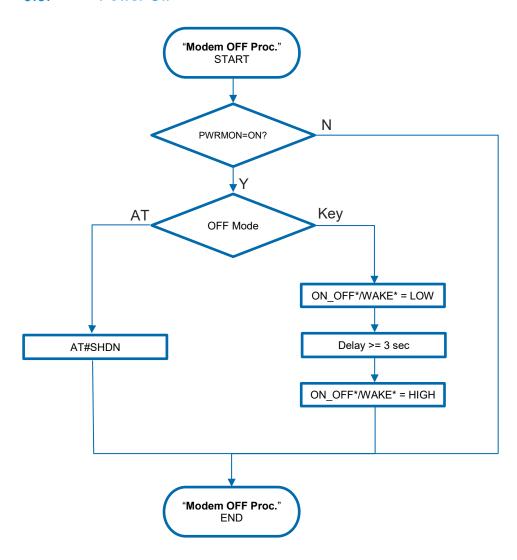


5.2. Power On





5.3. Power Off





5.4. Unconditional shutdown

This section will be available in next document revisions.

5.5. Wake from deep sleep mode

ME310G1 supports Power Saving Mode (PSM) functionality defined in 3GPP Release 12. When Periodic Update Timer expires, ME310G1 shuts down until the next scheduled wake-up time.

Asynchronous event controlled by host can wake up from deep sleep mode by asserting ON_OFF*/WAKE* pin LOW for at least 5 seconds.

Host can detect deep sleep mode by polling PWRMON pin if PSM has been previously configured.



5.6. Communication ports

5.6.1. USB 2.0 HS

The ME310G1 includes one integrated universal serial bus (USB 2.0 HS) transceiver.

The following table is listing the available signals:

| PAD | Signal | I/O | Function | NOTE |
|-----|--------|-----|---|------|
| U19 | USB_D+ | I/O | USB differential Data (+) | |
| V18 | USB_D- | I/O | USB differential Data (-) | |
| T18 | VUSB | Al | Power sense for the internal USB transceiver. | |

USB_VBUS input voltage range and input current are:

| Parameter | Min | Max |
|---|-------|-------|
| ABSOLUTE MAXIMUM RATINGS – NOT FUNCTIONAL | | |
| USB_VBUS Input level | -0.3V | 6.0V |
| Operating Range | | |
| USB_VBUS Input high level | 1.0V | 5.25V |
| USB_VBUS Input low level | 0V | 0.4V |

| Parameter | TYP |
|--------------------------|-----|
| CURRENT CHARACTERISTICS: | |
| USB_VBUS Input Current | 6uA |



5.6.2. SPI

The ME310G1 Module is provided by a standard 3-wire master or slave SPI interface with chip select control.

The following table is listing the available signals:

| PAD | Signal | I/O | Function | Type NOTE |
|-----|----------|-----|-----------------|--------------|
| AA5 | SPI_MOSI | I/O | SPI MOSI | CMOS 1.8V |
| Y8 | SPI_MISO | I/O | SPI MISO | CMOS 1.8V |
| AA7 | SPI_CLK | I/O | SPI Clock | CMOS 1.8V |
| Y6 | SPI_CS | I/O | SPI Chip Select | CMOS 1.8V |

5.6.3. Serial Ports

The ME310G1 module is provided with by 3 Asynchronous serial ports:

- Asynchronous Serial Port (USIF0)
- Asynchronous Serial Port (USIF1)*
- Auxiliary Serial Port

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 5V or other voltages different from 1.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work. On the ME310G1 the ports are CMOS 1.8.



NOTE:

*The USIF1 is currently NOT supported by ME310G1 firmware.



5.6.3.1. Asynchronous Serial Port (USIF0)

The serial port 0 on the ME310G1 is a +1.8V UART with 5 RS232 signals. It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

The following table is listing the available signals:

| RS232 Pin | Signal | Pad | Name | Usage |
|--------------|-----------|--|---------------------------|--|
| 2 | C104/RXD0 | AA15 | Transmit line | Output transmit line of ME310G1 UART |
| 3 | C103/TXD0 | Y16 | Receive line | Input receive of the ME310G1 UART |
| | | | | Pull-up default during ON state |
| 4 | DTR | (*) | Data Terminal Ready | Input to the ME910G1 that controls the DTE READY condition |
| 5 | GND | A3, A7, A9, A13, A17, B4, B6, B10, B12, B14, B16, C19, D18, F8, F12, F18, G19, H6, H14, J19, K18, M18, N19, P6, P14, T8, T12, U1, V2, W19, Y2, Y4 | Ground | Ground |
| 8 | C106/CTS0 | AA17 | Clear to Send | Output from the ME310G1 that controls the Hardware flow control |
| 7 | C105/RTS0 | Y18 | Request to Send | Input to the ME310G1 that controls the Hardware flow control Pull-up default during ON state |
| 9 | RING | (*) | Ring Indicator | Output from the ME910G1 that indicates the incoming call condition |

^{*} Alternate function with GPIO, refer to par. 5.7





NOTE:

According to V.24, some signal names are referred to the application side, therefore on the ME310G1 side these signal are on the opposite direction:

TXD on the application side will be connected to the receive line (here named C103/TXD0)

RXD on the application side will be connected to the transmit line (here named C104/RXD0)

For a minimum implementation, only the TXD, RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the ME310G1 when the module is powered off or during an ON/OFF transition (RESET included).

5.6.3.2. Asynchronous Serial Port (USIF1)

The serial port 1 on the ME310G1 is a +1.8V UART with 5 RS232 signals. It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

The following table is listing the available signals:

| RS232 Pin | Signal | Pad | Name | Usage |
|--------------|-----------|--|---------------|---|
| 2 | C104/RXD1 | AA11 | Transmit line | Output transmit line of ME310G1 UART |
| 3 | C103/TXD1 | Y12 | Receive line | Input receive of the ME310G1 UART Pull-up default during ON state |
| 5 | GND | A3, A7, A9, A13, A17, B4, B6, B10, B12, B14, B16, C19, D18, F8, F12, F18, G19, H6, H14, J19, K18, M18, N19, P6, P14, T8, T12, U1, V2, W19, Y2, Y4 | Ground | Ground |



| 8 | C106/CTS1 | Y14 | Clear to Send | Output from the ME310G1 that controls the Hardware flow control |
|---|-----------|------|--------------------|---|
| 7 | C105/RTS1 | AA13 | Request to Send | Input to the ME310G1 that controls the Hardware flow control |
| | | | | Pull-up default during ON state |

5.6.3.3. Auxiliary Serial Port

The auxiliary serial port on the ME310G1 is a CMOS 1.8V with only the RX and TX signals. The signals of the ME310G1 serial port are:

| PAD | Signal | I/O | Function | Туре | NOTE |
|-----|--------|-----|--------------------------------------|-----------|------|
| Y10 | TX_AUX | 0 | Auxiliary UART (TX Data to DTE) | CMOS 1.8V | |
| AA9 | RX_AUX | I | Auxiliary UART (RX Data from DTE) | CMOS 1.8V | |



5.7. General purpose I/O

The ME310G1 module is provided by a set of Configurable Digital Input / Output pins (CMOS 1.8V). Input pads can only be read; they report the digital value (high or low) present on the pad at the read time. Output pads can only be written or queried and set the value of the pad output.

An alternate function pad is internally controlled by the ME310G1 firmware and acts depending on the function implemented.

The following table shows the available GPIO on the ME310G1:

| PAD | Signal | I/O | Drive Strength | Default State | NOTE |
|-----|---------|-----|-------------------|-------------------|------------------------|
| V11 | GPIO_01 | I/O | 1 mA | INPUT - PD (100K) | |
| V13 | GPIO_02 | I/O | 1 mA | INPUT - PD (100K) | |
| D7 | GPIO_03 | I/O | 1 mA | INPUT - PD (100K) | |
| D9 | GPIO_04 | I/O | 1 mA | INPUT - PD (100K) | |
| D11 | GPIO_05 | I/O | 1 mA | INPUT - PD (100K) | Alternate function DTR |
| D13 | GPIO_06 | I/O | 1 mA | INPUT - PD (100K) | Alternate function |

5.7.1. Using a GPIO as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.



NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the ME310G1 when the module is powered off or during an ON/OFF transition.



5.7.2. Using a GPIO as OUTPUT

The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

5.8. External SIM Holder

Please refer to the related User Guide (SIM Holder Design Guides, 80000NT10001a).



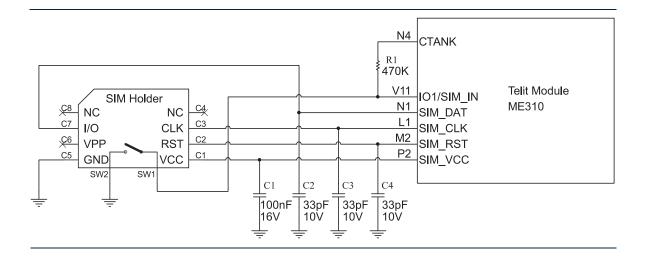
NOTE:

There is no dedicated signal (SIMIN) for "Presence SIM" in the ME310G1 pinout.

This feature can performed by connection of IO1 (Pad **V11**) or IO2 (Pad **V13**) or IO3 (Pad **D7**) or IO4 (Pad **D9**) or IO5 (Pad **D11**) or IO6 (Pad **D13**) to the switch embedded in the sim-holder.

SIM detection can be configured by specific AT Command.

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.





WARNING:

Pull-up 470K is required across CTANK (ball N4) and switch embedded in the sim-holder.



5.9. ADC Converter

The ME310G1 is provided by one AD converter. It is able to read a voltage level in the range of 0÷1.8 volts applied on the ADC pin input, store and convert it into 10 bit word.

The input lines are named as ADC (available on Pad B18).

The following table is showing the ADC characteristics:

| Item | Min | Typical | Max | Unit |
|---------------------|-----|---------|-----|------|
| Input Voltage range | 0 | - | 1.8 | Volt |
| AD conversion | - | - | 10 | bits |

5.9.1. Using ADC Converter

Available in a next document revision.

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

5.10. DAC Converter

The ME310G1 provides a Digital to Analog Converter. The signal (named DAC) is available on pin **R16** of the ME310G1.

5.10.1. Enabling DAC

Available in a next document revision.

5.11. CTANK

The ME310G1 provides an internal supply domain pin for additional capacitance or pullup reference to support only the specific use cases described in ME310G1 documentation. The internal supply domain (named CTANK) is available on pin **N4** of the ME310G1.

User application circuit should add a place-holder capacitor of 100uF 4V connected to pin **N4** of the ME310G1 to support an enhanced power loss recovering.

5.12. Forced USB boot

In some case of firmware upgrade FORCED_USB_BOOT pin must be set to 1.8V during poweron of ME310G1.

The input current is very low so 10K resistor to CTANK (pin N4) can be used to keep this pin in HI state.

FORCED_USB_BOOT pin must be connected only during firmware upgrade operation and normally it has to be left open.



FORCED_USB_BOOT and CTANK pins must be available in the user application circuit throught test points for easy connection of 10K resistor.



6. RF SECTION

6.1. Bands Variants

See section 2.2.

6.2. TX Output power

See section 2.5.

6.3. Antenna requirements

The antenna connection and board layout design are the most important aspect in the full product design as they strongly affect the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.

The antenna and antenna transmission line on PCB for a Telit ME310G1 device shall fulfil the following requirements:

| Item | Value |
|-----------------|--|
| Frequency range | Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s) |
| Bandwidth | 250 MHz in LTE Band 1 140 MHz in LTE Band 2, PCS1900 170 MHz in LTE Band 3, DCS1800 445 MHz in LTE Band 4 70 MHz in LTE Band 5, GSM850 80 MHz in LTE Band 8, GSM900 47 MHz in LTE Band 12 41 MHz in LTE Band 13 60 MHz in LTE Band 18 60 MHz in LTE Band 19 71 MHz in LTE Band 20 145 MHz in LTE Band 26 62 MHz in LTE Band 27 100 MHz in LTE Band 28 490 MHz in LTE Band 66 81 MHz in LTE Band 71 48 MHz in LTE Band 85 |
| Impedance | 50 ohm |



| Input power | ME310G1-W1: > 24dBm Average power ME310G1-WW: > 33dBm Average power | |
|-------------------|---|--|
| VSWR absolute max | ≤ 10:1 (limit to avoid permanent damage) | |
| VSWR recommended | ≤ 2:1 (limit to fulfill all regulatory requirements) | |

6.3.1. PCB Design guidelines

When using the ME310G1, since there's no antenna connector on the module, the antenna must be connected to the ME310G1 antenna pad by means of a transmission line implemented on the PCB.

This transmission line shall fulfil the following requirements:

| Item | Value |
|--------------------------|--|
| Characteristic Impedance | 50 ohm (+-10%) |
| Max Attenuation | 0.3 dB |
| Coupling | Coupling with other signals shall be avoided |
| Ground Plane | Cold End (Ground Plane) of antenna shall be equipotential to the ME310G1 ground pins |

The transmission line should be designed according to the following guidelines:

- Make sure that the transmission line's characteristic impedance is 50ohm;
- Keep line on the PCB as short as possible, since the antenna line loss shall be less than about 0.3 dB;
- Line geometry should have uniform characteristics, constant cross section, avoid meanders and abrupt curves;
- Any kind of suitable geometry / structure (Microstrip, Stripline, Coplanar, Grounded Coplanar Waveguide...) can be used for implementing the printed transmission line afferent the antenna;
- If a Ground plane is required in line geometry, that plane has to be continuous and sufficiently extended, so the geometry can be as similar as possible to the related canonical model;
- Keep, if possible, at least one layer of the PCB used only for the Ground plane; If possible, use this layer as reference Ground plane for the transmission line;
- It is wise to surround (on both sides) the PCB transmission line with Ground, avoid having other signal tracks facing directly the antenna line track.
- Avoid crossing any un-shielded transmission line footprint with other signal tracks on different layers;



- The ground surrounding the antenna line on PCB has to be strictly connected to the main Ground Plane by means of via holes (once per 2mm at least), placed close to the ground edges facing line track;
- Place EM noisy devices as far as possible from ME310G1 antenna line;
- Keep the antenna line far away from the ME310G1 power supply lines;
- If EM noisy devices (such as fast switching ICs, LCD and so on) are present on the PCB hosting the ME310G1, take care of the shielding of the antenna line by burying it in an inner layer of PCB and surround it with Ground planes, or shield it with a metal frame cover.
- If EM noisy devices are not present around the line, the use of geometries like Microstrip or Grounded Coplanar Waveguide has to be preferred, since they typically ensure less attenuation if compared to a Stripline having same length;



7. GNSS SECTION

ME310G1 module includes a state-of-art receiver that can simultaneously search and track satellite signals from multiple satellite constellations. This multi-GNSS receiver uses the entire spectrum of GNSS systems available: GPS, GLONASS, BeiDou, Galileo, and QZSS.

7.1. GNSS Signals Pin-out

| Pin | Signal | I/O | Function | Туре |
|-----|-------------|-----|-----------------------------|--------------|
| E19 | ANT_GNSS | I | GNSS Antenna (50 ohm) | |
| H18 | GNSS_LNA_EN | 0 | GNSS External LNA Enable | CMOS 1.8V |
| G16 | GNSS_1PPS | 0 | 1 Pulse per Second | CMOS 1.8V |

7.2. RF Front End Design

The ME310G1 Module doesn't contain the LNA needed to reach the maximum sensitivity. Active antenna (antenna with a built-in low noise amplifier) must be used and must be supplied with proper bias-tee circuit.

7.2.1. Guidelines of PCB line for GNSS Antenna

- Ensure that the antenna line impedance is 50ohm.
- Keep the antenna line on the PCB as short as possible to reduce the loss.
- Antenna line must have uniform characteristics, constant cross section, avoid meanders and abrupt curves.
- Keep one layer of the PCB used only for the Ground plane, if possible.
- Surround (on both the sides, over and under) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line of track.
- The ground around the antenna line on PCB has to be strictly connected to the Ground Plane by placing vias once per 2mm at least.
- Place EM noisy devices as far as possible from antenna line.
- Keep the antenna line far away from power supply lines.
- Keep the antenna line far away from GSM RF lines.
- If you have EM noisy devices around the PCB hosting the module, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.
- If you do not have EM noisy devices around the PCB hosting the module, use a strip-line on the superficial copper layer for the antenna line. The line attenuation will be lower than a buried one.



7.3. GNSS Antenna Requirements

GNSS active antenna must be used or integrated in the application.

7.3.1. GNSS Antenna specification

| ltem | Value |
|---------------------|---------------------|
| Frequency range | 1559.0 ~ 1610.0 MHz |
| Gain | 20 ~ 30dB |
| Impedance | 50 ohm |
| Noise Figure of LNA | < 1.5 (recommended) |
| DC supply voltage | DC 1.8 ~ 3.3V |
| VSWR | ≤ 3:1 (recommended) |

7.3.2. GNSS Antenna – Installation Guidelines

- The antenna must be installed according to the antenna manufacturer's instructions to obtain the maximum performance of GNSS receiver.
- The antenna location must be evaluated carefully if operating in conjunction with any other antenna or transmitter.
- The antenna must not be installed inside metal cases or near any obstacle that may degrade features like antenna lobes and gain.

7.3.3. Powering the External LNA (active antenna)

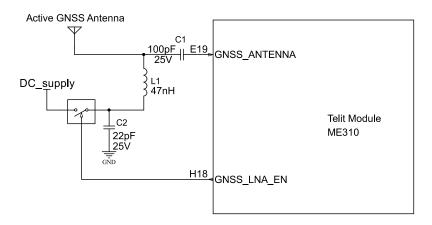
The LNA of active antenna needs a source of power because 1.8V or 3V DC voltage needed by active antenna is not supplied by the ME310G1 module, but can be easily included in the user application circuit.

The electrical characteristics of the GPS LNA EN signal are:

| Level | Min | Max |
|----------------------|------|------|
| Output High Level | 1.6V | 1.9V |
| Output Low Level | 0V | 0.3V |



Example of external antenna bias circuitry:



Be aware of max bias current in case of unwanted short on antenna cable because decoupling inductor can be damaged.

7.4. GNSS Characteristics

This section will be available in next document revisions.



8. AUDIO SECTION

The Telit digital audio interface (DVI) of the ME310G1 Module is based on the I²S serial bus interface standard. The audio port can be connected to end device using digital interface, or via one of the several compliant codecs (in case an analog audio is needed).

8.1. Electrical Characteristics

The product is providing the DVI on the following pins:

| Pin | Signal | I/O | Function | Internal Pull Up | Туре |
|-----|---------|-----|--|---------------------|-----------|
| C1 | DVI_WA0 | I/O | Digital Audio Interface (Word Alignment / LRCLK) | | CMOS 1.8V |
| D2 | DVI_RX | I | Digital Audio Interface (RX) | | CMOS 1.8V |
| E1 | DVI_TX | 0 | Digital Audio Interface (TX) | | CMOS 1.8V |
| F2 | DVI_CLK | I/O | Digital Audio Interface (BCLK) | | CMOS 1.8V |

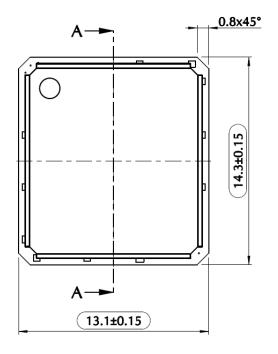
8.2. Codec examples

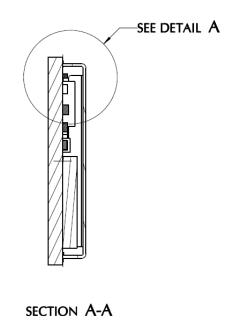
Please refer to the Digital Audio Application note.

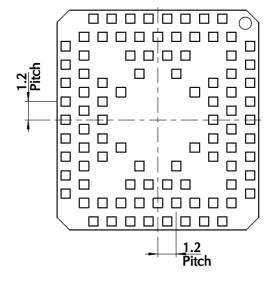
9. MECHANICAL DESIGN

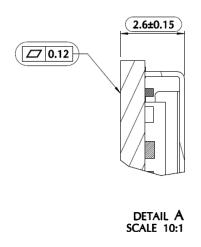
9.1. Drawing

9.1.1. ME310G1-W1











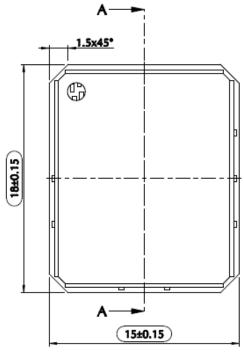
NOTE:

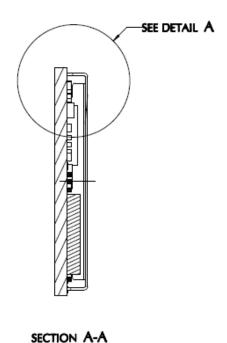
Dimensions in mm.

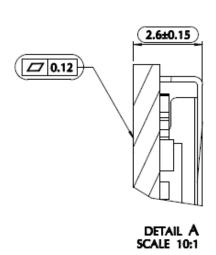
General Tolerance ± 0.1 , Angular Tolerance $\pm 1^{\circ}$, The tolerance is not cumulative.













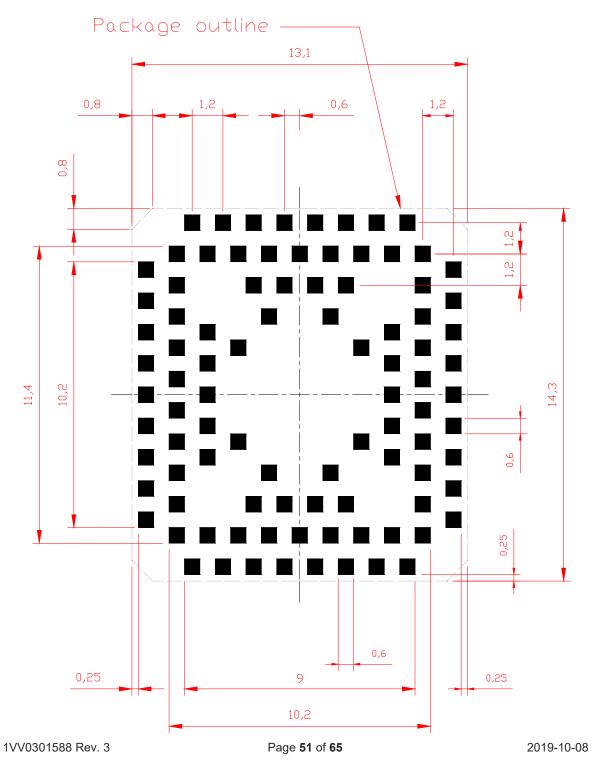
10. APPLICATION PCB DESIGN

The ME310G1 modules have been designed in order to be compliant with a standard lead-free SMT process.

10.1. Footprint

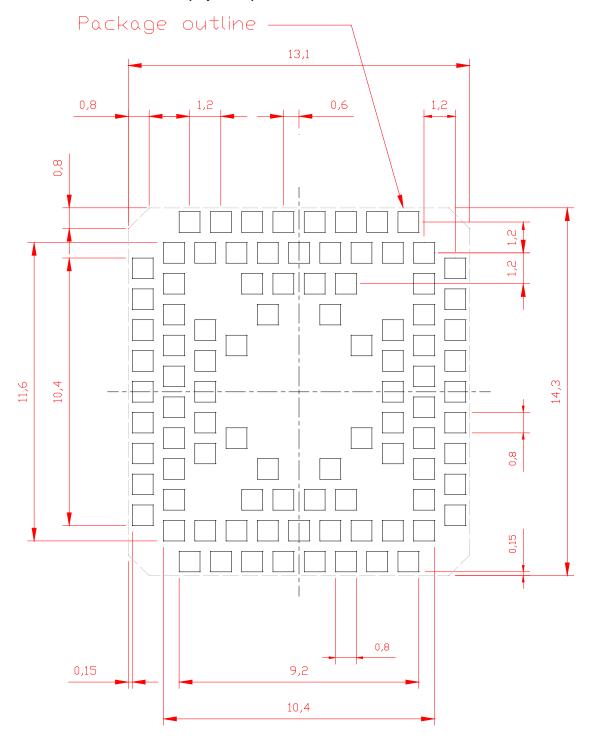
10.1.1. ME310G1-W1 and ME310G1-WW

COPPER PATTERN (top view)





SOLDER RESIST PATTERN (top view)

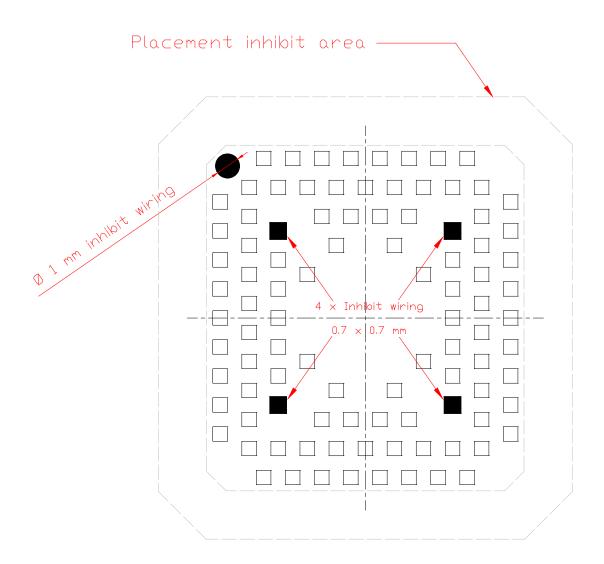




10.1.2. Recommendations for ME310G1-W1

In order to easily rework the ME310G1-W1 is suggested to consider on the application a 2 mm placement inhibit area around the module.

It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.





NOTE:

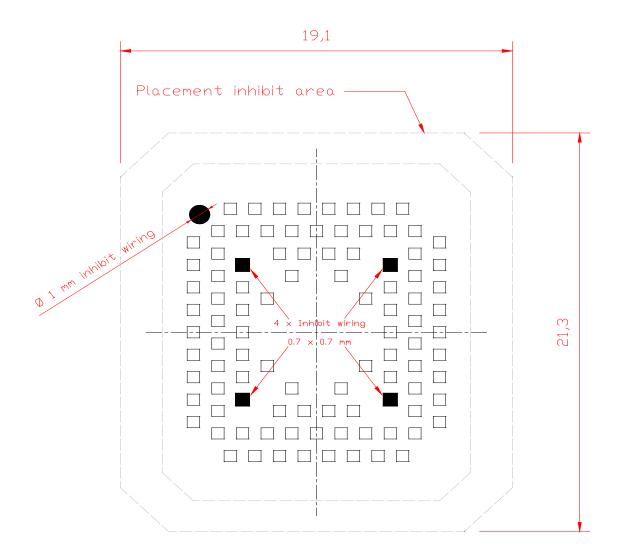
In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.



10.1.3. Recommendations for ME310G1-WW

In order to easily rework the ME310G1-WW is suggested to consider on the application placement inhibit area around the module as specified in the below figure.

It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.





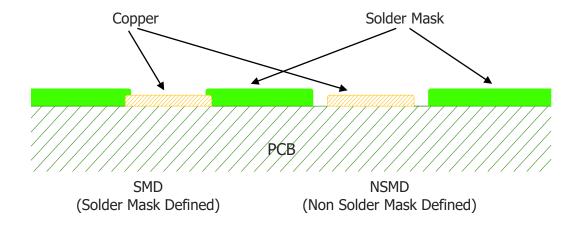
NOTE:

In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.



10.2. PCB pad design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



The recommendation for the PCB pads dimensions are 1:1 with module pads.

It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself

Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

| Finish | Layer Thickness (um) | Properties |
|-----------------------------------|----------------------|--|
| Electro-less Ni / Immersion Au | 3 –7 / 0.03 – 0.15 | good solder ability protection, high shear force values |

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

It is not necessary to panel the application's PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.



10.3. Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil \geq 120 μ m.

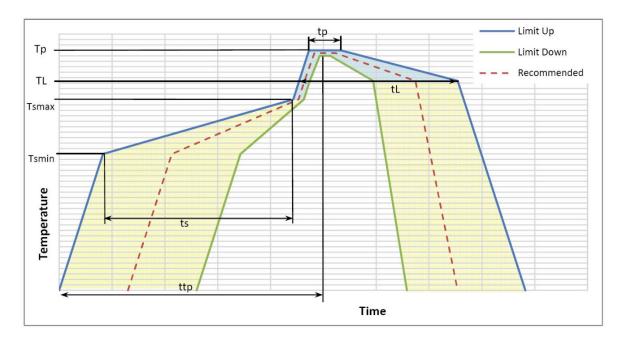
10.4. Solder paste

| Item | Lead Free |
|--------------|-----------|
| Solder Paste | Sn/Ag/Cu |

We recommend using only "no clean" solder paste in order to avoid the cleaning of the modules after assembly.

10.5. Solder Reflow

Recommended solder reflow profile:







WARNING:

The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customer must optimize the reflow profile depending on the overall system taking into account such factors as thermal mass and warpage..

| Profile Feature | Pb-Free Assembly |
|---|----------------------------------|
| Average ramp-up rate (T _L to T _P) | 3°C/second max |
| Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts) | 150°C 200°C 60-180 seconds |
| Tsmax to TL - Ramp-up Rate | 3°C/second max |
| Time maintained above: - Temperature (TL) - Time (tL) | 217°C 60-150 seconds |
| Peak Temperature (Tp) | 245 +0/-5°C |
| Time within 5°C of actual Peak Temperature (tp) | 10-30 seconds |
| Ramp-down Rate | 6°C/second max. |
| Time 25°C to Peak Temperature | 8 minutes max. |





NOTE:

All temperatures refer to topside of the package, measured on the package body surface



WARNING:

THE ME310G1 MODULES WITHSTANDS ONE REFLOW PROCESS ONLY.



11. PACKAGING

This section will be available in next document revisions.



12. CONFORMITY ASSESSMENT ISSUES

This section will be available in next document revisions.



13. SAFETY RECOMMENDATIONS

13.1. READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has

to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipment introduced on the market. All the relevant information's are available on the European Community website:

http://ec.europa.eu/enterprise/sectors/rtte/documents/

The text of the Directive 99/05 regarding telecommunication equipment is available, while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/



14. ACRONYMS

| LTE | Long Term Evolution | |
|-------|---|--|
| RF | Radio Frequency | |
| EMC | Electromagnetic Compatibility | |
| FDD | Frequency Division Duplexing | |
| EM | Electromagnetic | |
| EMI | Electromagnetic Interference | |
| РСВ | Printed Circuit Board | |
| USB | Universal Serial Bus | |
| HS | High Speed | |
| DTE | Data Terminal Equipment | |
| UMTS | Universal Mobile Telecommunication System | |
| WCDMA | Wideband Code Division Multiple Access | |
| HSDPA | High Speed Downlink Packet Access | |
| HSUPA | High Speed Uplink Packet Access | |
| UART | Universal Asynchronous Receiver Transmitter | |
| HSIC | High Speed Inter Chip | |
| SIM | Subscriber Identification Module | |
| SPI | Serial Peripheral Interface | |
| ADC | Analog – Digital Converter | |
| DAC | Digital – Analog Converter | |
| 1/0 | Input Output | |



| GPIO | General Purpose Input Output | |
|------|--|--|
| CMOS | Complementary Metal – Oxide Semiconductor | |
| MOSI | Master Output – Slave Input | |
| MISO | Master Input – Slave Output | |
| CLK | Clock | |
| DVI | Digital Voice Interface | |
| MRDY | Master Ready | |
| SRDY | Slave Ready | |
| CS | Chip Select | |
| RTC | Real Time Clock | |
| ESR | Equivalent Series Resistance | |
| VSWR | Voltage Standing Wave Radio | |
| VNA | Vector Network Analyzer | |
| PSM | Power Saving Mode according to 3GPP Rel.12 | |
| NAS | Non-Access Stratum | |



15. DOCUMENT HISTORY

| Revision | Date | Changes |
|----------|------------|---|
| 0 | 2019-03-11 | First issue |
| 1 | 2019-06-13 | Band list update, pinout update Added SIMIN, USB_VBUS, CTANK, PWRMON, FORCED_USB_BOOT pins description Added power on procedure |
| 2 | 2019-08-13 | Added ME310G1-WW Update of Temperature range table N16 pin update (ON_OFF*/WAKE*) ON/OFF procedure updated |
| 3 | 2019-10-02 | Added power consumption figures Added DTR and RING Removed B14 Update ME310G1-WW inhibit area reccomandation Extended Voltange Range lower limit change |

SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

www.telit.com



Telit Communications S.p.A. Via Stazione di Prosecco, 5/B I-34010 Sgonico (Trieste), Italy

Telit IoT Platforms LLC 5300 Broken Sound Blvd, Suite 150 Boca Raton, FL 33487, USA Telit Wireless Solutions Inc. 3131 RDU Center Drive, Suite 135 Morrisville, NC 27560, USA

Telit Wireless Solutions Co., Ltd. 8th Fl., Shinyoung Securities Bld. 6, Gukjegeumyung-ro8-gil, Yeongdeungpo-gu Seoul, 150-884, Korea Telit Wireless Solutions Ltd. 10 Habarzel St. Tel Aviv 69710, Israel

Telit Wireless Solutions Technologia e Servicos Ltda Avenida Paulista, 1776, Room 10.C 01310-921 São Paulo, Brazil

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